

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Yasuyuki Matsuya

Application No 10/663,282

Confirmation No.: 3218 .

Filed: September 16, 2003

Art Unit: 2615

For: Data Communication Method, Data
Transmitting Apparatus, Data Receiving
Apparatus, And Data Transmission Program

Examiner: Walter F. Briney III

DECLARATION UNDER 37 C.F.R. §1.132

1. I am named inventor and applicant for patent in U.S. patent application Serial Number 10/663,282. I hold a Doctor Degree in Electrical Engineering and I have worked in the circuit design of data communications field for 30 years.
2. I understand that the United States Patent Examiner, in an Office Action mailed November 28, 2007, has suggested that we should submit a Declaration to supply evidence in support of our arguments previously made. I am therefore providing this Declaration in accordance with the Examiner's request.
3. Attached to this Declaration is a set of "Reference Diagrams" which I herewith submit as evidence together with the following testimony to traverse the Examiner's rejection and to further substantiate our explanation of why our invention is different from the cited prior art (e.g., Sulavuori). A brief description of these Reference Diagrams next follows:
 - a. Reference Diagram 1 is a fair and accurate depiction of how conventional transmission using PCM-A/D conversion is accomplished;
 - b. Reference Diagram 2 is a fair and accurate depiction of a PCM-A/D conversion transmitter-receiver pair, illustrating how in conventional transmission using PCM-A/D conversion the transmitter requires a parallel-to-serial converter and a frame processor that inserts preambles, and the receiver requires a frame processor for detecting

preambles and for performing clock synchronization and a serial-to-parallel converter.

- c. Reference Diagram 3 is a fair and accurate depiction of delta A/D conversion on which CVSD scheme disclosed in Sulavuori is based (for example, column 4, lines 6-12, column 4, lines 53-67 and column 5 lines 1-17, and column 7, lines 28-39, of Sulavuori).
- d. Reference Diagram 4 is a fair and accurate depiction illustrating that it is not necessary for the delta A/D conversion to provide the parallel-to-serial converter and the frame processor at the transmitter shown in Reference Diagram 2 and the frame processor and the serial-to-parallel converter at the receiver shown in Reference Diagram 2.
- e. Reference Diagram 5 is a fair and accurate depiction of an exemplary waveform produced when using delta A/D conversion;
- f. Reference Diagram 6 is a fair and accurate depiction of how a delta A/D conversion system (on which the CVSD scheme disclosed in Sulavuori is based) will narrow the width of pulses to be transmitted by a pulse shaper at the transmitter;
- g. Reference Diagram 7 is a fair and accurate depiction of an exemplary waveform produced when using delta A/D conversion, illustrating how the average shifts from the middle of a high level and a low level to the low level side, thereby resulting in a DC offset;
- h. Reference Diagram 8 is a fair and accurate depiction of a DC feedback circuit, discussed more fully in the explanation below.
- i. Reference Diagram 9 is a fair and accurate depiction of the structure of a noise-shaping A/D converter;
- j. Reference Diagram 10 is a fair and accurate depiction of a transmitter and a receiver that use noise shaping modulation.

Our invention employs noise shaping with return-to-zero (RZ) signals

- 4. A major feature of the invention as recited in independent claims 1 and 2 is that a noise shaping method is combined with the use of return-to-zero (RZ) signals, which provides the advantage of reducing jitter. In contrast, Sulavuori does not disclose or suggest the feature of the invention as recited in claims 1 and 2. Indeed, Sulavuori is unaware of reducing jitter as a problem to be solved.
- 5. It appears that the Examiner considers that a continuously variable slope delta modulation (CVSD) of Sulavuori corresponds to the noise shaping method recited in claims 1 and 2 (page 2, item 1, line 5 of the current office action). However, the CVSD is fundamentally different from applicants' noise shaping method, as will be next demonstrated. Please refer to the accompanying "Reference Diagrams" which compare the Sulavuori technique with Applicants' technique.

6. In the set of included Reference Diagrams, Diagram 1 is included for background understanding of how conventional transmission using PCM-A/D conversion is accomplished and is believed to be self-explanatory. The Sulavuori technique is introduced beginning with Reference Diagram 3; applicants' noise-shaping technique is introduced beginning with Reference Diagram 9.

The CVSD technique of Sulavuori

1. As noted above, Reference Diagram 3 shows delta A/D conversion on which CVSD scheme disclosed in Sulavuori is based (for example, column 4, lines 6-12, column 4, lines 53-67 and column 5 lines 1-17, and column 7, lines 28-39, of Sulavuori).
2. At a transmitter, in order to convert the voltage of an input signal at point B, the input signal is differentiated to obtain the difference between the voltage at point A and the voltage at point B, the difference voltage is converted into k-bit binary data, the converted binary data is further converted into a serial data stream, and the resultant stream is transmitted. At a receiver, an original k-bit signal is restored from a serial data stream received, and the restored k-bit signal is added to data corresponding to the voltage at point A which has already been obtained to reproduce data corresponding to the voltage at point B.
3. Unlike the conventional transmission using PCM-A/D conversion, transmission, using delta A/D conversion allows reproducing data from the transmitter precisely by setting a sampling rate to a sufficiently high value as compared with the signal band, even if k is set to one. In this case, unlike the conventional transmission using PCM-A/D conversion in which each group contains a plurality of pieces of bit data, each group contains one bit data, so that it is not necessary to detect the head and tail of data in each group. Thus, data corresponding to an original signal can be obtained by adding current data to an integrated value of a plurality of pieces of data that have been already transmitted by that time.
4. As shown in Reference Diagram 4, it is not necessary for the delta A/D conversion to provide the parallel-to-serial converter and the frame processor at the transmitter shown in Reference Diagram 2 and the frame processor and the serial-to-parallel converter at the receiver shown in Reference Diagram 2.
5. However, because of the characteristics of the employed conversion technique, the delta A/D conversion requires an integrator at the receiver that integrates received data in order to reproduce data corresponding to an original signal. In other words, the delta A/D conversion cannot reproduce the original signal unless such an integrator is installed.

6. In addition, integrators have theoretically an infinite amplification factor with respect to a DC offset. Thus, when a DC offset is present in received data, the integrators overflow or underflow and they cannot operate even if the offset is considerably small.
7. Here, the ground level at the receiver is determined by an average of signals of a low level and signals of a high level. Furthermore, a difference between this average and the middle of a low level and high level results in a DC offset.
8. In the delta A/D conversion, the frequency of occurrence of "1" contained in data is the same as that of "0" for a long period of time. Thus, if such data is transmitted and the duty ratio of a pulse is 100% as shown in Reference Diagram 5, the average is equal to the middle of a low level and a high level. As a result, the difference becomes zero and signal waveforms having no DC offsets can be obtained. Integrators do not overflow even if such signal waveforms are input thereto.
9. However, as shown in Reference Diagram 6, Sulavuori narrows the width of pulses to be transmitted (see FIG. 1 of Sulavuori) by a pulse shaper at the transmitter (for example, reference numerals 105 and 210 shown in FIG. 4A and 4B), thereby resulting in a difference between the duration of a high level in a signal corresponding to logical value "1" and the duration of a low level in a signal corresponding to logical value "0". As a result, as shown in Reference Diagram 7, the average shifts from the middle of a high level and a low level to the low level side, thereby resulting in a DC offset. Therefore, upon receiving such a signal waveform, integrators underflow and cannot operate.
10. As shown below, there are two solutions to solve this problem.
11. Instead of directly inputting a received signal into the integrator, a pulse expander provided in the receiver restores the duty ratio of a pulse of the received signal to 100% so as to cancel the DC offset, and the resultant pulse is input into the integrator.
12. As shown in Reference Diagram 8, a DC feedback circuit comprised by a low pass filter having a small time constant is added to the integrator to set a DC amplification factor to one, thereby preventing overflow and underflow being generated.
13. However, the low pass filter used for the DC feedback circuit is implemented by a first-order RC circuit. Thus, in the solution (2), in order to obtain a sufficient amplification factor so as to allow the integrator operating at a 20Hz, which is the lowest frequency in the audible frequency band, it is necessary to set the cut-off frequency of the low pass filter to 0.02 Hz or below. Therefore, extremely large size elements must be provided for a capacitor C2 and a

resistor R2 shown in Reference Diagram 8, making it difficult to miniaturize the receiver. In addition, a resistor R1 and a capacitor C2 serve as a low pass filter, and thus the integrator cannot perform an integration operation.

14. As described above, it is indispensable for Sulavuori to provide the pulse expander in the receiver that expands the duty ratio of a pulse to 100%. In addition, it is necessary for this pulse expander to precisely restore the duty ratio of a pulse to 100%.

A/D Conversion using noise-shaping method of present invention

15. As shown in Reference Diagram 9, the structure of a noise-shaping A/D converter resembles the structure of a delta A/D converter shown in Reference Diagram 3. However, by providing an integrator in a loop at a transmitter, the noise-shaping A/D converter provides distinctive features which are quite different from the delta A/D conversion.
16. As explained above, in the transmission using delta A/D conversion, the transmitter differentiates a signal, quantizes the differentiated signal, and transmits the quantized signal, and the receiver integrates received signals and smoothes the integrated signal using a low pass filter to reproduce an original signal.
17. In contrast, as shown in Reference Diagram 10, in the transmission using noise-shaping A/D conversion, the transmitter integrates a signal, quantizes the integrated signal, differentiates the quantized signal, and transmits the differentiated signal. The receiver shapes the waveforms of a received signal using an inverter, and smoothes the shaped signal to reproduce an original signal.
18. Here, the noise shaping modulation at the transmitter shown in Reference Diagram 10 corresponds to a process recited in the first paragraph of Claim 1, a 1-bit conversion section recited in Claim 2. Moreover, an inverter, a resistor, and a capacitor at the receiver shown in Reference Diagram 10 correspond to a process recited in the last paragraph of Claim 1 and a drive section recited in Claim 8.
19. In this way, the transmission using noise-shaping A/D conversion requires no integrator at the receiver. Therefore, even if a DC offset is present in a signal input to the receiver, neither overflow nor underflow takes place since no integrators are provided in the receiver. As a result, even if the transmitter converts a signal into a return-to-zero signal having a narrow pulse width, it is not necessary for the receiver to expand the pulse width of a received signal. That is, the receiver requires no pulse expander. Therefore, it is possible to simplify the structure of the drive section recited in Claim 8 that does not include an integrator and a pulse expander. In these respects, the transmission using noise-shaping A/D conversion is superior to the transmission using delta A/D conversion.

Comparison of Applicants' Invention and Sulavuori

20. As can be understood from the comparison between Reference Diagram 2 and 10, the structures of a transmitter and a receiver in the conventional transmission using PCM-A/D conversion are quite different from those in the transmission using noise-shaping A/D conversion according to the present invention.
21. In addition, although Sulavuori superficially resembles the present invention in respect of combining a coder and a pulse shaper, advantageous effects obtained by the present invention in which a coder employs noise-shaping A/D conversion is significantly different from the effect obtained by Sulavuori in which a coder employs delta A/D conversion. Moreover, as can be understood from the comparison between Reference Diagrams 6 and 10, the structure of the receiver is quite different between Sulavuori and the present invention.
22. The Examiner asserts that the invention as recited in independent claims 1 and 2 (hereinafter referred to as "the present invention") is rejected under 35 U.S.C. 102(b) as being anticipated by Sulavuori et al. because, for example, the CVSD of Sulavuori et al. is the same as the noise-shaping A/D conversion of the present invention.
23. However, as explained above in detail, the CVSD of Sulavuori et al. is different from the noise-shaping A/D conversion of the present invention. Therefore, the present invention is not anticipated by Sulavuori et al.
24. Furthermore, the present invention and Sulavuori are quite different in respect of effects obtained by narrowing the pulse width. Sulavuori allows data multiplexing by narrowing the pulse width (column 3, lines 31-47). In contrast, the present invention can suppress jitter which may be generated when a receiver shapes signal waveforms (page 10, second paragraph, of the original specification).
25. Specifically, the present invention employs the transmission using noise-shaping A/D conversion. Thus, even if the width of a pulse to be transmitted is narrowed, the receiver requires no pulse expander and integrator, and the receiver can reproduce an original signal by simply shaping the waveform of a received signal by an inverter, etc. Thus, narrowing the pulse width at the transmitter is quite effective to solve the problem in which noise is generated by a variation in the width of a pulse reproduced at the receiver that is caused by a variation in a threshold level (i.e., the averages shown in Reference Diagrams 5 and 7) in the waveform shaping (page 5, line 16, through page 6, line 20, of the original specification).
26. In contrast, in the transmission using delta A/D conversion as employed in Sulavuori, since an integrator overflows if a signal whose waveform has been

shaped by an inverter, etc., is directly input to the integrator, the receiver expands the duty ratio of a pulse of the signal to 100% and then integrates the expanded pulse. That is, the duty ratio of the pulse is always 100% regardless of the width of a pulse transmitted from the transmitter and a variation in width of a reproduced pulse due to a variation in a threshold level at the receiver. Therefore, in the transmission using delta A/D conversion as employed in Sulavuori, narrowing the width of a pulse is absolutely irrelevant to suppressing noise due to the jitter.

27. Moreover, the transmission using delta A/D conversion is quite different from the transmission using noise-shaping A/D conversion in respect of a driving scheme of a speaker.
28. In Sulavuori, transistors that form an operational amplifier, etc., used in the integrator at the receiver, operate in the saturated region, so that output impedance is generally high. As a result, it is impossible to drive a speaker having low input impedance. Thus, in order to drive such a speaker, it is necessary to provide an A-class power amplifier having low power efficiency that amplifies an output from the integrator.
29. In contrast, as explained above, in the transmission using noise-shaping A/D conversion as employed in the present invention, the receiver can reproduce the original signal at the transmitter based on signals obtained by, for example, shaping waveforms of a received signal using an inverter. Furthermore, transistors that form the inverter, etc., operate in the non-saturated region, so that output impedance is low. Thus, it is possible to directly drive a speaker having low input impedance using an output from the inverter, etc. This is a D-class operation that can realize excellent power efficiency.
30. In this manner, the circuit structure of the present invention in which the receiver requires neither a pulse expander nor an integrator and the advantageous effects obtained by such a structure are quite different from those in Sulavuori.

Further Response Regarding the Examiner's Comments on Applicants' Arguments

31. I understand that the Examiner is reading "noise shaping" to mean a technique that includes "a feedback loop that includes a measure of the error encountered by quantizing a signal input to the quantizer: $y(n)=x(n)+E(x(n-1))$ —Eq. (1)." [Examiner's Office Action page 8]. I also understand that the Examiner is construing the term CVSD to mean "a delta modulation scheme that quantizes the difference between an input sample and a previously quantized input sample; and that the Examiner considers the output of the quantizing element is fed back to the input of the quantizer after a subtraction element subtracts the quantizer output from a currently input sample— $y(n)=x(n)-Q(x(n-1))$ —Eq. (2); $Q(x(n-1))=x(n-1)+E(x(n-1))$ —Eq. (3); $y(n)=x(n)-x(n-1)-E(x(n-1))$ —Eq. (4). I further understand that the Examiner thus concludes by comparing Eq. (1) with Eq. (4) that the output of a CVSD filter is the difference between a noise-shaped current sample and the previous sample; and for this reason the CVSD A/D converter appears to perform noise-shaping. [Examiner's Office Action page 8].

32. My response to the Examiner's observation is as follows:

The Wikipedia entry cited by the Examiner with respect to noise shaping (i.e., reference U cited by the Examiner) states that ". . . noise shaping is a bit reduction technique used to minimize quantization error" (emphasis added: see page 1, first paragraph, line 1 of Wikipedia entry). As is well known in the art, $\Delta\Sigma$ modulators decrease a quantization error in a frequency range which is lower than a sampling frequency of the $\Delta\Sigma$ modulators, and thus the $\Delta\Sigma$ modulators perform noise shaping.

On the other hand, when a signal converted by means of Δ modulators such as those employing CVSD is demodulated at a receiver side, a quantization error having an original spectrum is also demodulated. Therefore, the CVSD is not noise shaping.

In order to facilitate the Examiner's understanding, I have prepared the following explanations based on an excerpt from an English reference ("Understanding Delta-Sigma Data Converters", Richard Schreier et al., Wiley-IEEE Press, November 2004, pp. 4-10), which is well known in the art of A/D converters.

An output signal of Δ modulators is expressed by Equation (1.2) shown below.

$$v(n) = [u(n) - u(n-1)] + [e(n) - e(n-1)] \quad (1.2)$$

where v denotes an output signal, u denotes an input signal, and e denotes a quantization error.

That is the Δ modulators output a difference value (i.e., differential value) of the

input signal and a difference value (i.e., differential value) of the quantization error. The original input signal can be demodulated by inputting this output signal to an integrator. However, in demodulating the original input signal, the original quantization error is restored at the same time. That is, the $\Delta\Sigma$ modulators do not minimize the quantization error, and thus they do not perform noise shaping.

By the way, as stated above, an integrator is required to demodulate an output signal of Δ modulators such as those employing the CVSD. In contrast, as explained in the reference, an output signal of $\Delta\Sigma$ modulators is expressed by Equation (1.3) shown below.

$$v(n) = u(n-1) + [e(n) - e(n-1)] \quad (1.3)$$

That is, the output signal includes an input signal itself. Therefore, no integrators are required in demodulating an output signal of the $\Delta\Sigma$ modulators (noise shaping). It is sufficient for a receiver to provide only a low pass filter that eliminates a quantization error in a frequency range which is higher than a sampling frequency.

As described above, the CVSD employed by Sulavuori is different from the noise shaping method of the invention as recited in independent Claims 1 and 2 (hereinafter referred to as "the present invention"). Therefore, the present invention would not have been anticipated by Sulavuori. In addition, dependent Claims 3-5 and 8-13 would not have been anticipated by Sulavuori at least by virtue of their dependency to the independent claims.

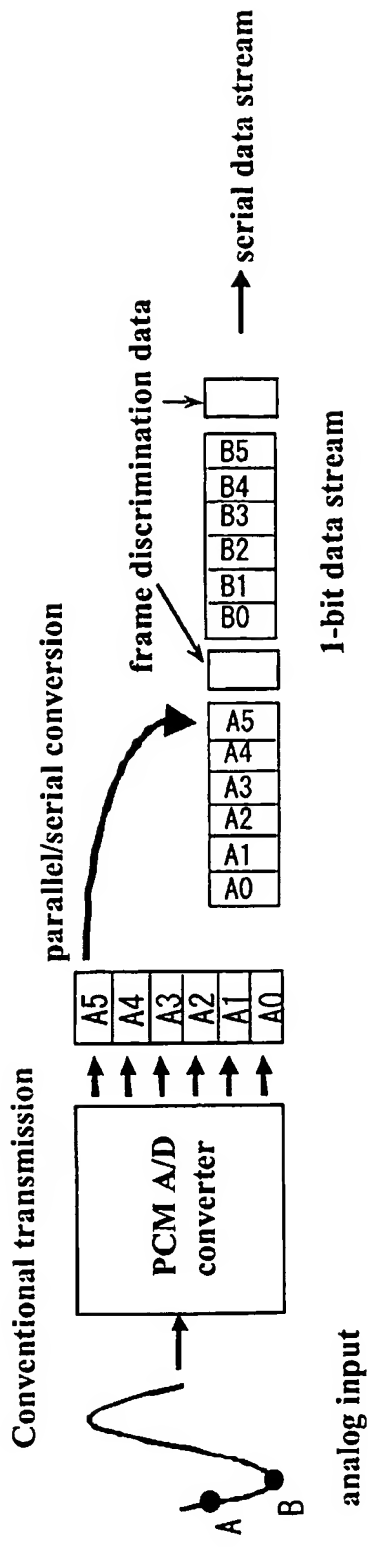
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or Imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Inventor's signature: Yasuyuki Matsuya

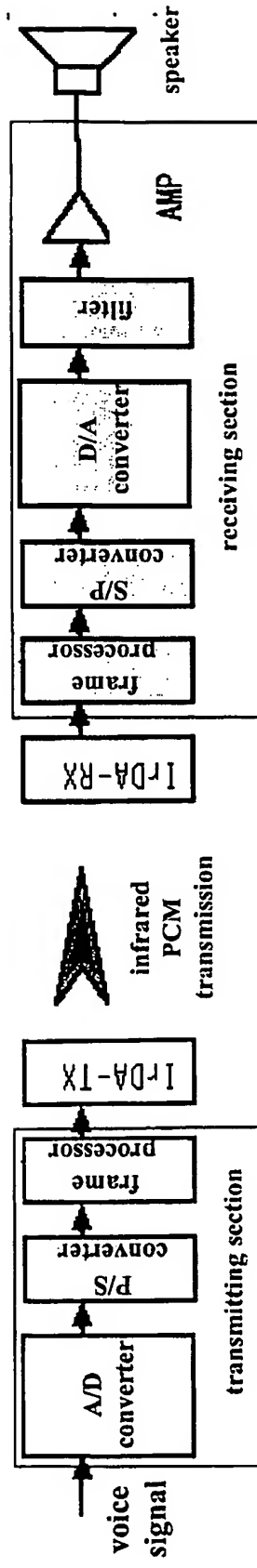
Yasuyuki Matsuya

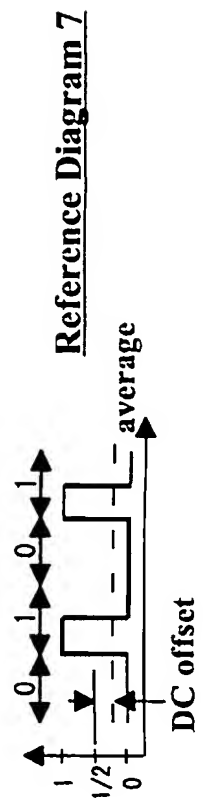
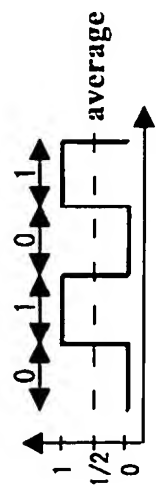
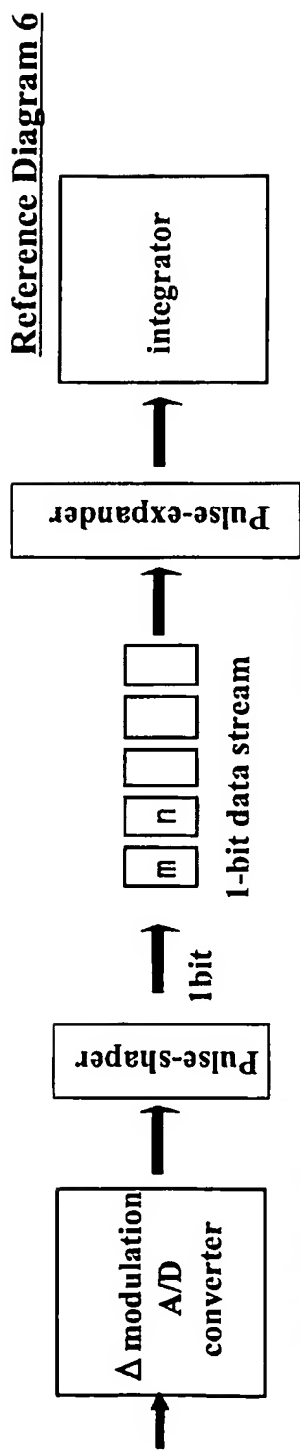
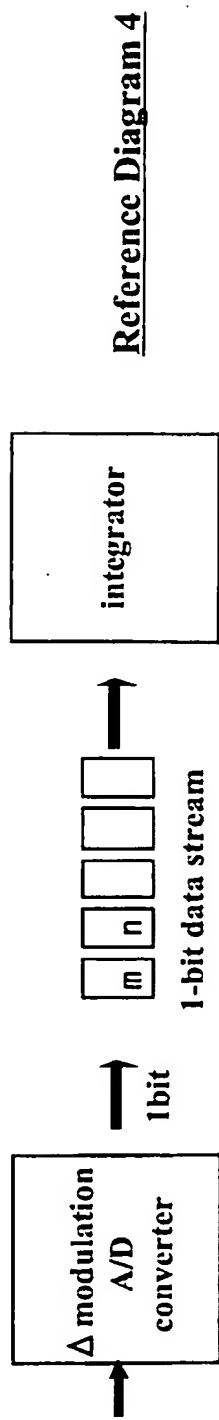
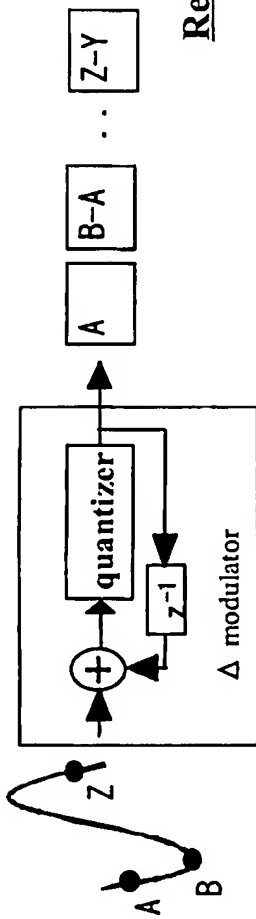
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Reference Diagram 1

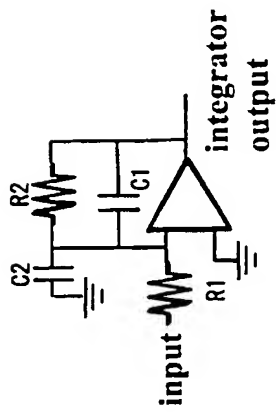


Reference Diagram 2

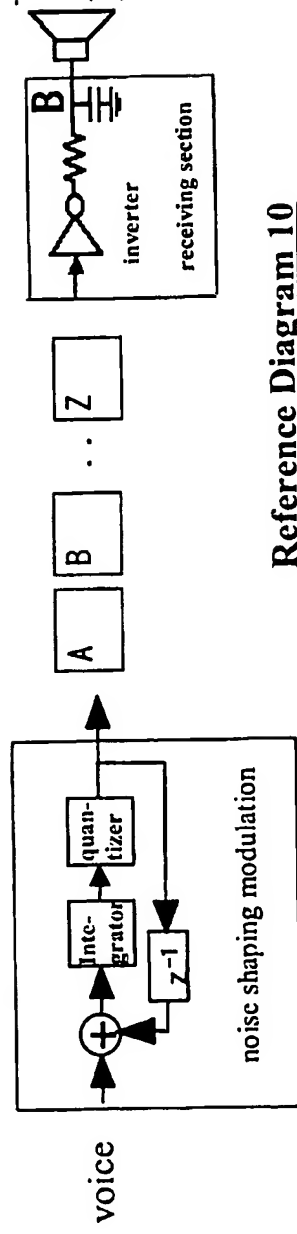
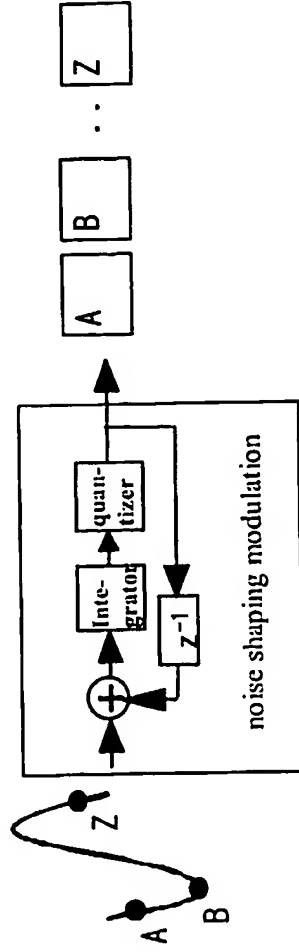




Reference Diagram 8



Reference Diagram 9



Reference Diagram 10

and generate each output utilizing all preceding input values. Thus, the converter incorporates memory elements in its structure. This property destroys the one-to-one relation between input and output samples. Now only a comparison of the complete input and output waveforms can be used to evaluate the converter's accuracy, either in the time or in the frequency domain.

A common measure of a converter's accuracy is the signal-to-noise ratio (SNR) for a sine-wave input. The relationship between ENOB and SNR for an ideal Nyquist converter with sine-wave excitation is $SNR = 6.02ENOB + 1.76$. The inverse relationship is often applied to oversampling converters to convert an SNR into an effective number of bits.

As will be shown in later chapters, the implementation of oversampling converters requires a considerable amount of digital circuitry, in addition to some analog stages. Both need to be operated faster than the Nyquist rate. However, the accuracy requirements on the analog components are relaxed compared to those associated with Nyquist-rate converters. The cost paid for high accuracy thus includes faster operation and added digital circuitry; both of these are getting cheaper as digital IC technology advances. Hence, oversampling converters are gradually taking over in many applications previously dominated by Nyquist-rate ones.

1.2 Delta and Delta-Sigma Modulation

Next, oversampling analog-to-digital converters processing *baseband signals* (i.e. signals with spectra centered around dc) will be discussed. Such data converters contain several stages. Analog and digital filter stages may be used before and after the stage (called the *modulator*, or *converter loop*) which performs the actual analog-to-digital conversion. The two main types of oversampling modulators are the *delta* modulator and the *delta-sigma* modulator. Fig. 1.3a shows a basic delta modulator used as an ADC. It is a feedback loop, containing an internal low-resolution ADC and DAC, as well as a loop filter (here, an integrator). It is a nonlinear system (due to the quantizing effect of the ADC) as well as a dynamic one (due to the memory in the integrator), and hence its analysis is a difficult mathematical task. Simple qualitative understanding of its operation can, however, be gained by using a linearized model of the internal ADC which consists of a unity-gain buffer and

an additive quantization noise e . Assuming perfect operation of the DAC as well as a reference voltage $V_{ref} = 1$ V and a sampling rate $f_s = 1$ Hz, the discrete-time linear system of Fig. 1.3b results. Analyzing this, it can easily be shown that the (digital) output signal at time n (i.e. $t = n/f_s$) is

$$v(n) = u(n) - u(n-1) + e(n) - e(n-1). \quad (1.2)$$

The name *delta modulator* is derived from the fact that the output is based on the difference (delta) between a sample of the input and a predicted value of that sample. In the general case, the loop filter may be a higher-order circuit, which generates a more accurate prediction of the input sample $u(n)$ than $u(n-1)$, to subtract from the actual $u(n)$. This type of modulator is sometimes called a *predictive encoder*.

The advantage of this structure is that for oversampled signals the difference $(u(n) - u(n-1))$ is much smaller than $u(n)$ itself, on average, and hence larger input signals can be allowed. There are, however, several disadvantages. The loop filter (integrator for the first-order loop shown) is in the feedback path, and hence its nonidealities limit the achievable linearity and accuracy. Also, in the demodulator, a DAC and a demodulation filter (for first-order modulators, an integrator) are

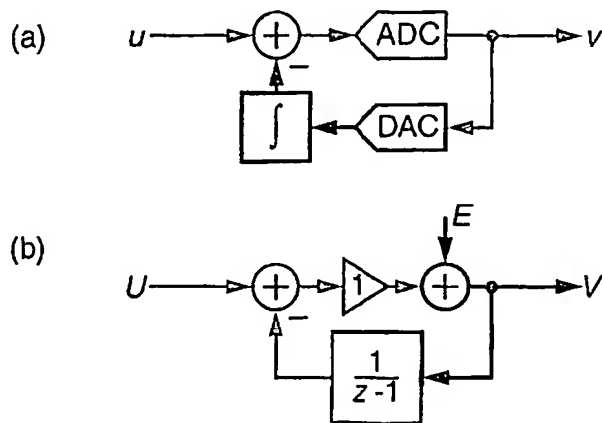


Figure 1.3: (a) A delta modulator used as an ADC and (b) its linear z -domain model.

needed. The filter has a high gain in the signal band, and hence will amplify the nonlinear distortion of the DAC as well as any noise picked up by the signal between the modulator and demodulator.

An alternative oversampling structure which avoids the shortcomings of the predictive modulator is shown in Fig. 1.4a. It is again a feedback loop, containing a loop filter as well as an internal low-resolution ADC and DAC, but the loop filter is now in the forward path of the loop. Replacing as before the quantizer (ADC) by its linear model, the linear sampled-data system of Fig. 1.4b results. Analysis gives

$$v(n) = u(n-1) + e(n) - e(n-1). \quad (1.3)$$

Thus, the digital output contains a delayed, but otherwise unchanged replica of the analog input signal u , and a differentiated version of the quantization error e . Since the signal is not changed by the modulation process, the demodulation operation does not need an integrator as was the case for the delta modulator. Hence, the amplification of in-band noise and distortion at the receiver does not take place. Furthermore, the differentiation of the error e suppresses it at frequencies which are small compared to the sampling rate f_s . In general, if the loop filter has a high gain in the signal band, the in-band quantization "noise" is strongly attenuated, a process now commonly called *noise shaping*.

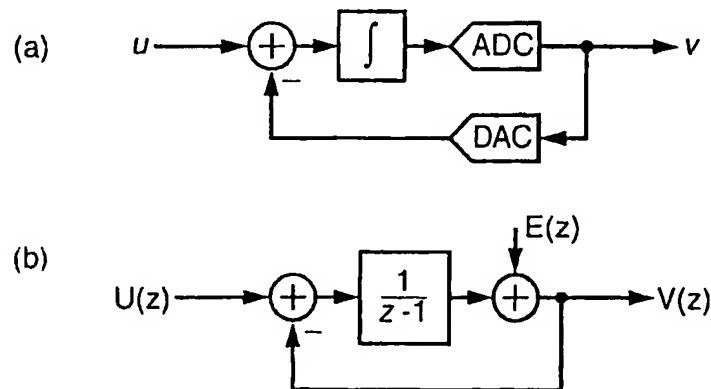


Figure 1.4: (a) A delta-sigma modulator used as an ADC and (b) its linear z -domain model.

Any nonlinearity of the ADC is simply combined with the quantization error e , and is thus suppressed in-band along with e . Nonlinear distortion in the DAC, however, affects the output signal without any shaping, and hence it represents a major limitation on the attainable performance. This effect can be handled in various ways. The simplest, and historically earliest, method is to use single-bit quantization. In this case, the input/output characteristic of the DAC consists of only two points, and hence the DAC's operation is inherently linear.[†] For multi-bit (typically, 2-5 bit) quantization, digital correction or dynamic matching techniques may be used. These will be discussed in Chapter 5.

It can be shown that the system of Fig. 1.4 can be obtained from that of Fig. 1.3 by cascading an integrator or summing block with the delta modulator. Hence, the structure of Fig. 1.4 came to be called a *sigma-delta* ($\Sigma\Delta$) *modulator*. Alternatively, one can observe the differencing at the input, followed by the summation in the loop filter, and hence call the structure a *delta-sigma* ($\Delta\Sigma$) *modulator*. Both terms have been used in the past to denote the first-order system of Fig. 1.4 with a single-bit quantizer. Other systems with higher-order loop filters, multi-bit quantizers, etc. are most properly called *noise-shaping modulators*, but it is common to extend the term $\Delta\Sigma$ modulator (or $\Sigma\Delta$ modulator) to these systems as well. This text follows the accepted usage. Examples of these general $\Delta\Sigma$ modulator systems will be briefly discussed in the next section.

The output noise due to the quantization error in the $\Delta\Sigma$ modulator is $q(n) = e(n) - e(n-1)$, as (1.3) shows. In the z -domain, this becomes $Q(z) = (1 - z^{-1})E(z)$, and in the frequency domain, after z is replaced by $e^{j2\pi fT}$, the *power spectral density* (PSD) of the output noise is found to be

$$S_q(f) = (2 \sin(\pi fT))^2 S_e(f). \quad (1.4)$$

†. More precisely, the DAC operation is *affine*, rather than linear. Since the input-output behavior of a memoryless binary DAC can be represented exactly by $w = kv + c$, where k is the DAC gain and c is the DAC offset, a binary DAC is linear (in the strict sense of the term) only if $c = 0$. However, since the dc offset of a converter is often immaterial, the distinction between an affine DAC and a truly linear DAC is usually unimportant.

Here, $T = 1/f_s$ is the sampling period, and $S_e(f)$ is the 1-sided PSD of the quantization error (noise) of the internal ADC. For "busy" (i.e., rapidly and randomly varying) input signals, one may approximate e with white noise of mean-square value $e_{rms}^2 = \Delta^2/12$ where Δ is the step size of the quantizer, and thus

$$S_e(f) = \frac{\Delta^2}{6f_s}. \quad (1.5)$$

The filtering function $1 - z^{-1}$ is called the *noise transfer function* (NTF). The squared magnitude of the NTF as a function of frequency is illustrated in Fig. 1.5.

As Fig. 1.5 illustrates, the NTF of the $\Delta\Sigma$ modulator is a highpass filter function. It suppresses e at frequencies around 0, but the NTF also enhances e at higher frequencies around $f_s/2$.

We introduce next the *oversampling ratio*

$$OSR = \frac{f_s}{2f_B}. \quad (1.6)$$

where f_B is the maximum signal frequency, i.e. the signal bandwidth. OSR defines how much faster we sample in the oversampled modulator than in a Nyquist-rate converter.

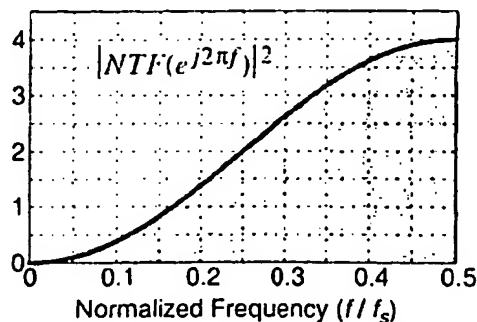


Figure 1.5: Noise-shaping function for the $\Delta\Sigma$ modulator shown in Fig. 1.4.

Integrating $S_q(f)$ between 0 and f_B gives the in-band noise power. By (1.4)-(1.6), and assuming $OSR \gg 1$, to a good approximation

$$q_{rms}^2 = \frac{\pi^2 c_{rms}^2}{3(OSR)^3}. \quad (1.7)$$

As expected, the in-band noise decreases with increasing OSR . However, this decrease is relatively slow: doubling the OSR reduces the noise only by 9 dB, and hence enhances the ENOB by only about 1.5 bits. Even for $OSR = 256$, $ENOB < 13$ bits results, assuming single-bit quantization is used.

1.3 Higher-Order Single-Stage Noise-Shaping Modulators

An obvious way to increase the resolution (i.e., the ENOB) of the $\Delta\Sigma$ modulator is to use a higher-order loop filter. By adding another integrator and feedback path to the circuit of Fig. 1.4, the structure of Fig. 1.6 results. Linearized analysis gives

$$V(z) = z^{-1}U(z) + (1 - z^{-1})^2 E(z). \quad (1.8)$$

This indicates that the NTF is now $(1 - z^{-1})^2$ in the z -domain, which applies a shaping function of $(2 \sin(\pi f T))^4$ to the PSD of e . It follows that the in-band noise power is (to a good approximation for $OSR \gg 1$)

$$q_{rms}^2 = \frac{\pi^4 c_{rms}^2}{5(OSR)^5}. \quad (1.9)$$

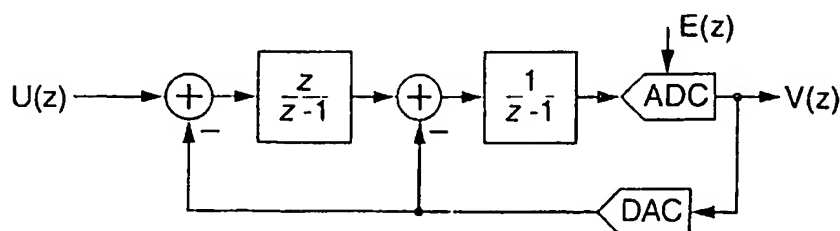


Figure 1.6: A second-order delta-sigma modulator.

Hence, doubling OSR results in about 2.5 bits of additional resolution. This is a much more favorable trade-off than that of the first-order modulator. For example, if we assume that single-bit quantization with $\Delta = 2$ results in $e_{rms}^2 = 1/3$, (1.9) indicates that ENOB is about 19 bits for $OSR = 256$, whereas a first-order modulator only achieves an ENOB of about 13 bits under the same assumptions. (Chapter 3 will show that this simple comparison is slightly flawed because a second-order single-bit modulator exhibits *quantizer overload* and thus has $e_{rms}^2 > 1/3$. A more accurate value is 17 ENOB for $OSR = 256$. Despite this 2-bit discrepancy, the ENOB of a second-order modulator does increase by 2.5 bits for each doubling of OSR .)

In principle, by adding more integrators and feedback branches to the loop, even higher-order NTFs can be obtained. For an L^{th} -order loop filter resulting in $NTF(z) = (1 - z^{-1})^L$, the in-band noise power is approximately

$$q_{rms}^2 = \frac{\pi^{2L} e_{rms}^2}{(2L + 1)(OSR)^{2L + 1}} \quad (1.10)$$

and the number of bits added to the resolution by doubling the OSR is given by $L + 0.5$. The in-band noise as a function of OSR based on (1.10) is plotted in Fig. 1.7. Here 0 dB corresponds to a quantization noise power of e_{rms}^2 .

For high-order loops, stability considerations, which have thus far been ignored, reduce the achievable resolution to a lower value than that given by the above equations and Fig. 1.7. For high-order, single-bit modulators the difference is substantial, amounting to more than 60 dB for a 5th-order modulator. This topic will be discussed in detail in Chapter 4.

1.4 Multi-Stage (Cascade, MASH) Modulators

An increasingly popular structure, which eases the stability problems associated with high-order modulators, is the *cascade* modulator, also called the *multi-stage* or *MASH* (for Multi-stAge noise-Shaping) modulator. The basic concept is illustrated in Fig. 1.8. The output signal of the first stage is given by